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TOTAL PAGES (including Cover Page) 7 DATE: September 23, 2003

Assistant Commissioner for Patents  
TO: Attn.: Examiner Paresh H. Patel FROM: Mr. James R. Foley, Reg. No. 39,979

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**NOTES:** Applicant: Daniel B. D'Souza  
For: WAFER LEVEL DYNAMIC  
BURN IN  
Serial No. 09/918,183  
Filed: July 30, 2001  
Art Unit: 2829  
Examiner: Paresh H. Patel  
Ref.: 00-464

**CERTIFICATION OF FACSIMILE TRANSMISSION**

I hereby certify that this paper is being facsimile transmitted to the Patent  
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In re application of: Daniel B. D'Souza

Serial No.: 09/918,183

Filed: July 30, 2001

For: WAFER LEVEL DYNAMIC BURN IN

COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Transmitted herewith is a Response to the Office Action Mailed July 30, 2003 for the above-identified application.

The filing fee has been calculated as shown below:

	(Col. 1)		(Col. 2)	(Col. 3)
	Claims Remaining After Amendment		Highest No Previously Paid for	Present Extra
TOTAL	* 5	MINUS	** 20	0
INDEP.	* 1	MINUS	** 3	0
<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEP. CLAIM				

SMALL ENTITY	
Rate	Addit. Fee
x 9 =	\$ .00
x 42 =	\$ .00
+ 130 =	\$ .00
TOTAL ADDIT. FEE	\$ .00

OR

OTHER THAN A SMALL ENTITY	
Rate	Addit. Fee
x 18 =	\$ .00
x 84 =	\$ .00
+ 260 =	\$ .00
TOTAL	\$ .00

OR

- \* If the entry in Col. 1 is less than the entry in Col. 2, write "0" in Col. 3.  
 \*\* If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, write "20" in this space.  
 \*\*\* If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, write "3" in this space.

The "Highest Number Previously Paid For" (Total or independent) is the highest number found from the equivalent box in Col. 1 of a prior amendment or the number of claims originally filed.

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☒ The Commissioner is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. 12-2252.

- ☒ Any filing fees required under 37 CFR 1.16 for the presentation of extra claims.  
☒ Any patent application processing fees under 37 CFR 1.17

Dated: September 23, 2003

  
 James R. Foley, Reg. No. 39,979  
 Attorney of Record

PATENT

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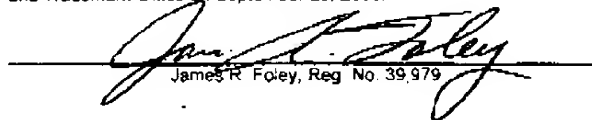
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Serial No.: 09/918,183 )  
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BURN IN )  
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Applicant: D'Souza )  
)  
Attorney Ref: 00-464 )

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James R. Foley, Reg. No. 39,979

RESPONSE TO OFFICE ACTION MAILED JULY 30, 2003

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450  
Mail Stop Non-Fee Amendment

Sir:

In the matter of the above-identified application and in response to the Office Action mailed July 30, 2003, kindly consider the following amendment and remarks toward reconsideration of the present application. The Office Action was indicated as being final, and the present Response is being filed within two months of the mailing date of the Office Action.

**AMENDMENTS**

Please amend the claims as follows:

1. (Currently amended) A wafer comprising:

a plurality of DRAM dies on the wafer, wherein each DRAM die has a test data in pad and a test data out pad; and

conductive connections interconnecting the test data out and test data in pads of the DRAM dies, said conductive connection providing that said DRAM's can be burned-in on the wafer, wherein the DRAM dies on the wafer are arranged in rows, wherein each row comprises a plurality of DRAM dies and each DRAM die in a given row is daisy chained to the next DRAM die in the row, wherein the last DRAM die in a row is daisy chained to the first DRAM die in the next row via a metal line on a scribe area of the wafer, wherein the DRAM dies on the wafer are connected to power busses along a scribe area so that the dies can be powered.

2. (Original) The wafer as recited in claim 1, wherein the DRAM dies are IEEE1149.1 (JTAG) compliant, and include the following pads: TDI (Test Data In), TDO (Test Data Out), TCK (Test Clock) and TMS (Test Mode Set).

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3. (Original) The wafer as recited in claim 2, wherein the TDO pad of each DRAM die is connected to the TDI pad of the next DRAM die on the wafer.

4. (Original) The wafer as recited in claim 2, wherein the TMS and TCK pads of the DRAM dies are connected in parallel.

5. (Original) The wafer as recited in claim 4, wherein the TMS and TCK pads of the DRAM dies are connected via metal lines running along a scribe area of the wafer.

6. (Canceled)

7. (Canceled)

8. (Canceled)

9. (Canceled)

10-20. (Withdrawn)

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